A Leakage Power Reduction Technique in Nanoscale Circuit Design

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Abstract: As the in semiconductor industries progress by adapting the Moore's law faithfully from many decades to enhance the booming market of the semiconductor devices which reduces the overall dimension of the device. The objective of this research is to find out the run time leakage reduction technique for CMOS devices for development of semiconductor industries, In over proposed work a novel technique for leakage reduction is introduce here Diode sleep transistor which are external controlling transistor are incorporated between PUN and PDN during working condition both PMOS and NMOS diode transistor are in Cut off region which results in more resistive path for the digital circuits, and rail the digital circuits from supply voltage to mitigate the leakage power, without any scarification of the performance of the digital circuits. Here we have implemented a novel approach for mitigation of static power by introducing the sleep and pass transistor logic in between PUN and PDN to provide more resistive path. All the simulation is performed by SPICE simulator by using 32nm technology and calculate the leakage at different operating temperature 25^0C and 110^0C with C_L=1pF at 100MHz frequency.

Key Words: **Low power consumption, Shorter Channel Effect, PDP, DSM technology.**

1. INTRODUCTION

As per the Moore's Law, the size of the wafer is reduces day by day to develop the electronics world and overall the density per unit area is also doubled as the size of the devices reduced in every year as a result the consumption of the power increases on a single IC due to millions of the transistor fabrication. There are three main factor which effects the overall power dissipation in MOS circuit design i.e the contribution of all the power is the main aspects to enhance the performance of the device [1-3]. If we talk about the low power VLSI circuit design technique, we follow the two types of the device dimension reduction that is scaling of voltage constantly and scaling the field constantley. Dynamic power consumption effects the power supply, If the power reduces significantly, it improves the overall robustness in digital circuits. Most of the researcher is going on reduction of the dynamic and static power dissipation which increases drastically with supply voltage scaling. The propagation delay increases [1, 4], due to the reduction in the f_{clk} and lower transistor current. The critical path of the supply voltage cannot be alter due to the speed constant of design. To avoid this problem, multi V_{DDH} is given to critical path and the supply voltage is scale down for non-critical path [3,4]. For interfacing in the circuit to communicate among each other, due to the different voltage level [5], Here in this graph there is drastic increases in the static version of the power without degrading overall performance of the circuit.

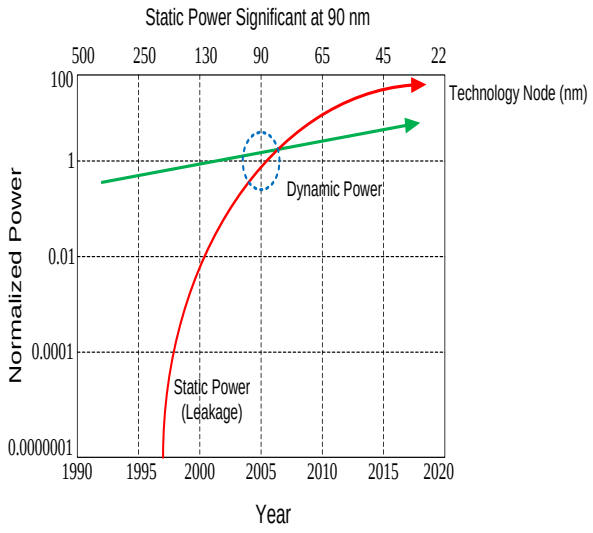


Fig.1. Enchantment of leakage power with scaling of technology in Intel Chip.

2.1 Literature Review Of Performance Evaluation Parameters

Leakage power flow in the transistor in ideal condition when transistor is in OFF condition. The current which flow in ideal condition is I_{SUB} and I_{Gate} leakage current. The total leakage current is contributed by all types of leakage current.

This type of leakage current flow in the transistor or reverse bias PN diode is formed between well and substrate. The main contribution of reverse bias PN junction diode in which current flows quite close to the layer of valance and conduction band which flow due to minority carrier which is not a major role player in channel modulation of the digital. As the electron and hole pairs generate inside the depletion regions of when this condition appears reverse bias junction leakage currents. When input vector applied to the circuit then input signal of CMOS inverter is high, there is a reverse potential difference of V_{DD} is formed between n-well and drain terminal, which results in flow of reverse diode leakage current through the drain junction as shown in Fig. 2. Another type of the dominants mode arises in the common mode of the current flow inside the circuit is in the form of leakage power which has to be suppressed to increase the reliability of the circuit.

In MOS transistor, proper capacitance is generated by which silicon oxide (SiO_2) layer at Gate terminal very good insulator, but as the thickness of Sio_2 layer is reduces the electrons can tunnel across very small thickness in insulation layer. The probability of this tunnelling drops off exponentially with increasing of oxide thickness. This Gate oxide tunnelling current is represented the I_{ON} and I_{OFF} current is the major contributors in the low power VLSI circuit design so as to increase the robustness of the circuit as shown in Fig. 2.

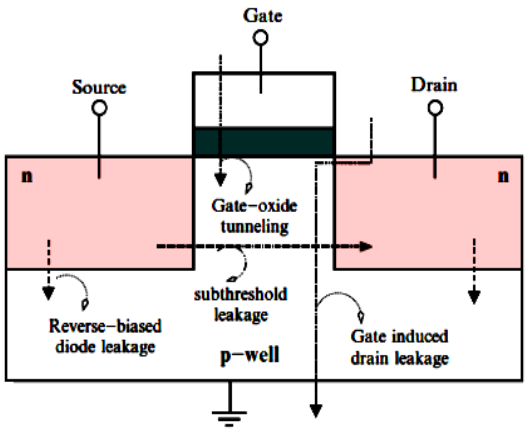


Fig. 2: Components of Leakage Power Dissipation [2]

The main effect from which sub threshold current flows basically consist of three reasons: DIBL effect, another is weak inversion

effect and which bring the two well quite closer to each other in this condition no electrons will flow from drain terminal to source terminal is cause by increasing the drain voltage which reduces the threshold voltage of the transistor. The major role is played in channel engineering is the depletion region which is created in between P and N type semiconductor devices the drain voltages which help in increases with the help of gate terminal voltage. The main responsibility is to balance the electron in depletion region is more on drain voltage rather than gate voltage. Hence the charge present on gate terminal voltage attracts larger number carriers in to the channel for balancing the charges inside the depletion region. With the drastic increase in the drain current channel gate shorter with the actual channel which results in the increasing the static power while bringing the two wells closer to each other [48].

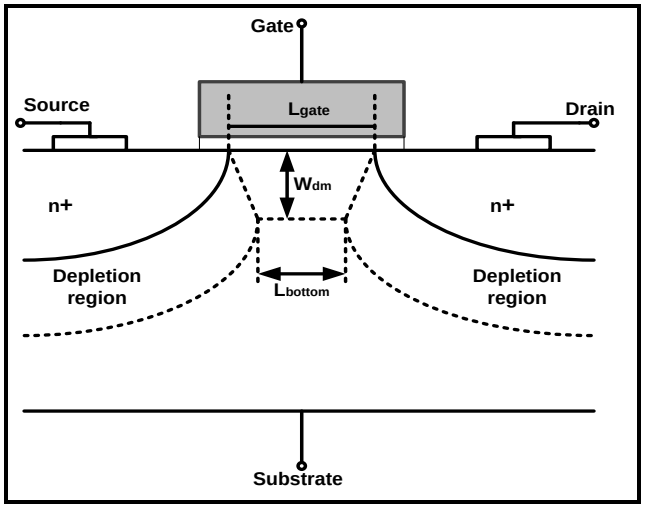


Fig.3: NMOS transistor of the depletion regions in short channel device

Second reason which helps in causing for increase of sub-threshold current is weak inversion effect inside the transistor. When we apply gate voltage is which is below the threshold voltage ($V_{GS}< V_T$) , charge carriers which move by diffusion along the surface. This weak inversion effect which occur when gate to source voltage is smaller than threshold voltage which have significant role in total power consumption in low power circuit design. Another type of effect is known as Punch-through condition, there is Punch-through of electrons and hole take place between drain and source terminal. This occur when source and drain depletion region come closer to each other and try to touch deep in the channel[6-8].

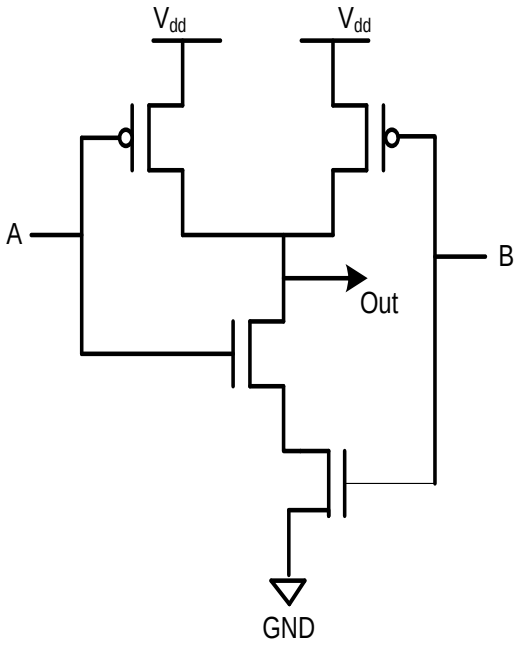
These two powers aforementioned, namely switching power and short circuit power account for the dynamic power consumption. These power consumptions can be reduced by lowering supply voltage below the threshold voltage. In such case the leakage energy balances the active energy dissipation [5], [6]. However, excessive reduction in the power supply results in degradation in performance and eventually increases the circuit performance variation. As compared with deep subthreshold operation, near-threshold operation has been considered to be more practical because it implies substantially improved performance and variation with comparable reduction in power.

To mitigate leakage current in CMOS circuits, several leakage reduction techniques hhas been propsed by different researchs. These techniques are based on concept of Multiple Supply Voltage, Multiple Threshold Voltage,

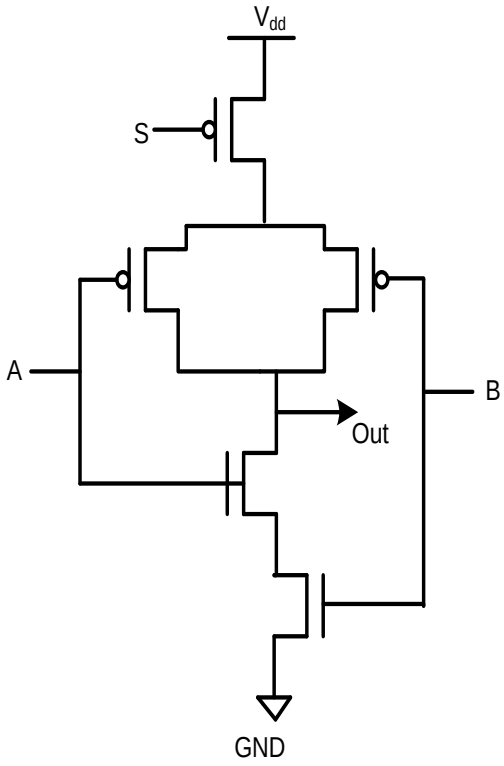
Adaptive Body Biasing, Transistor Stacking and Power Gating [12-14, 16].

Jing Yang and Yong-Bin Kim, 2013, In this paper author proposed a new type self-adaptive RBB system by using reverse body bias technique for minimization of leakage power adaptively by comparing main type of leakage current like sub-threshold (I_{SUB}), Gate tunnelling (I_{GTL}), The comparison results are shown in Table containing mean and standard deviation (SD) of output and power dissipation. From this table it can be concluded that type I level shifter has 1.56% low mean in output voltage and 21.5 times less mean and 21.76 times less deviation in power dissipation [15].

Oleg Semenov et. al., 2002, MN1 will be turned ON, and MP1 will be turned OFF. Since the input is also connected to MN3, hence it will be turned ON. As a result the output will be high logic. In case of input logic is low, MN1 and MN3 will be turned OFF. But MP1 will be turned ON. Hence the high logic will be applied to gates of MN4 and MN5 transistors, which will turn them ON. This high logic will be applied to MN2, which will turn it ON..



(a)



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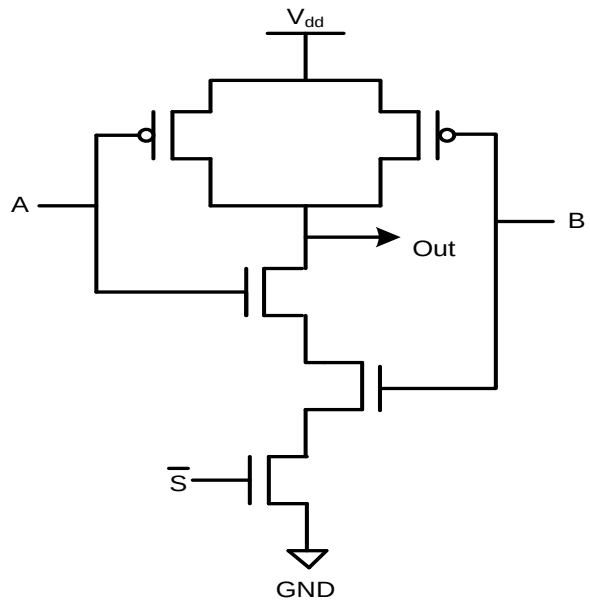

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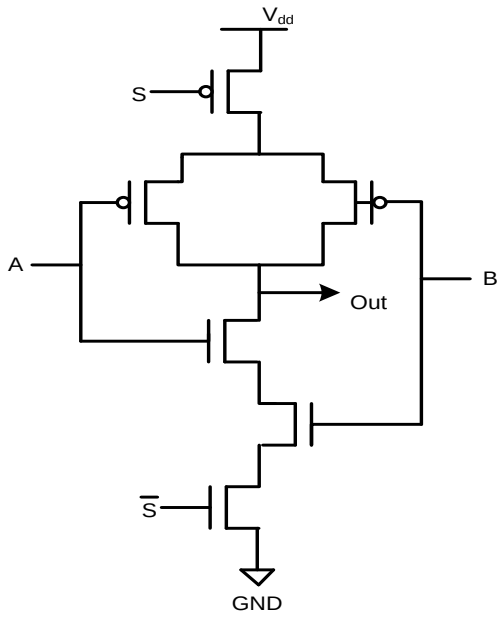
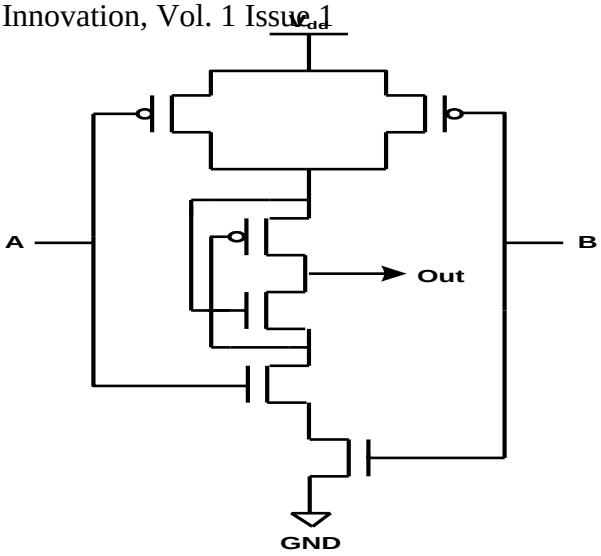


(d)

III. PROPOSED WORK

Here we have introduce a new designees for mitigation of leakage with various combinations namely DOIND approach with the help of the transistor known, Diode Header Sleep (DHS), Diode Footer (LFS) and Diode Header Footer (DHFS), for increasing the resistance of the devices for further mitigation of the leakage



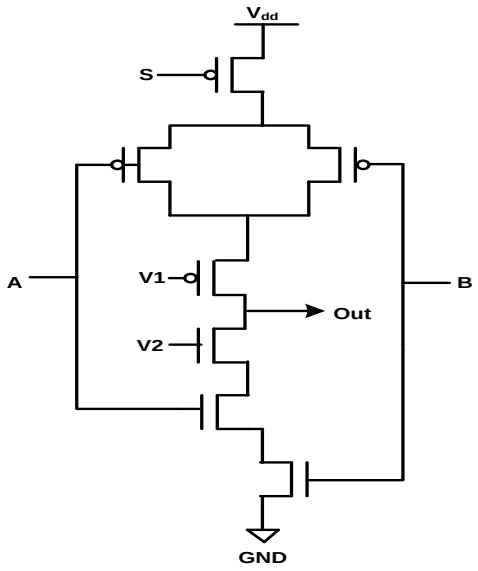
power. These combinations are likely to be external controlling technique for further

Figure.4: The conventional NAND Gate (NG) is shown and the leakage mitigation techniques are introduced is known as LECTOR with various combinations.

reduction in power consumption. Among various dynamic standby and run time power reduction techniques, dynamic voltage scaling is one of the techniques for designing low power deep submicron circuits. This reduces not only dynamic but static power as well. Voltage level shifter is one of the key components of such circuits which can fulfill aforementioned requirements. Power reduction is the main aim to increases the overall life of the battery b y this can be save during run time so as to achieve minimum switching activity take place when clock signal is applied to both PMOS and NMOS transistor is known as dynamic power dissipation.

Proposed DHS, DFS and DHFS is made by using two input NAND gate as shown in Figure. 5. (a), (b) and (c). Here the circuit is inserted in between the PUN and PDN to increases maximum resistance so, that minimum current

can flow, which is helpful in enhancing the life of the battery operated device. The working is quite similar to that of NAND gate at all input vector combination 00,01, 10 and 11. The maximum leakage flow in 11 condition and least leakage will flow at 00 condition, conventional circuit is facing more leakage than techniques which are introduce in between the NAND gate and generate the proper logic of the design. During 00 condition voltage at Node N1 is 1 in active condition but in ideal condition voltage is 0 because it disconnect from V_{DD} in order to suppress the leakage power. Which is followed by 01 and 10 condition but in 11 condition reverse process is happened.



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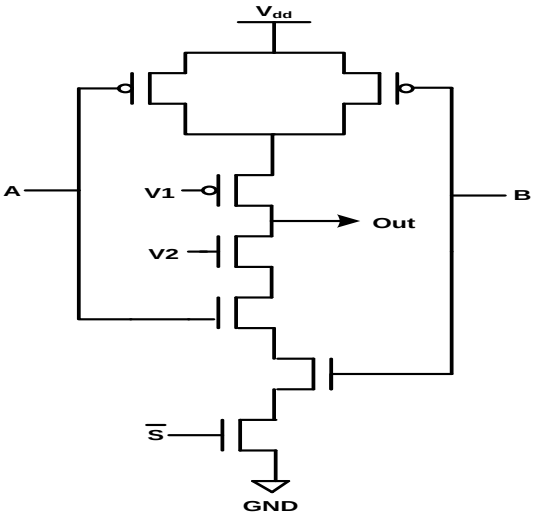

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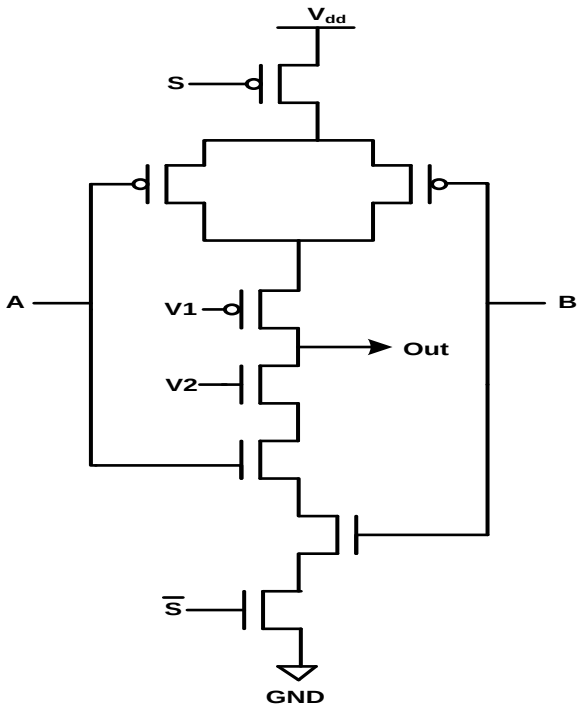

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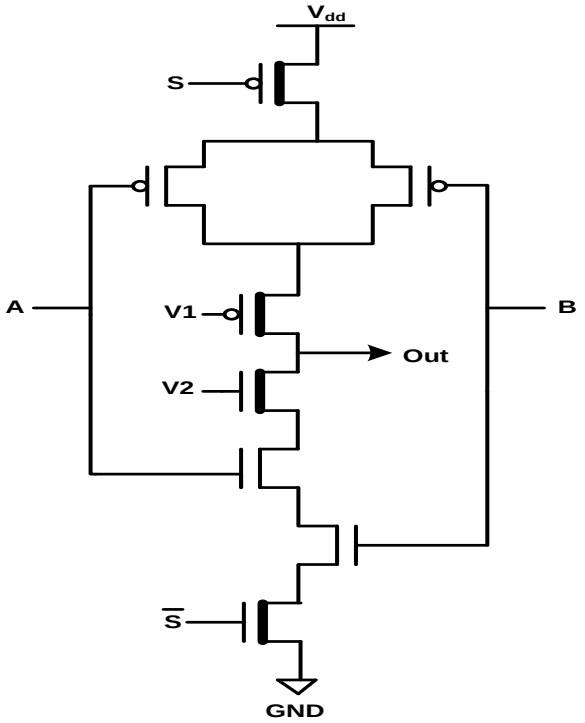

(d)

Fig.5: A New Proposed techniques (a) DHS (b) DFS and (c) DHFS Low Vth (d) DHFS High Vth

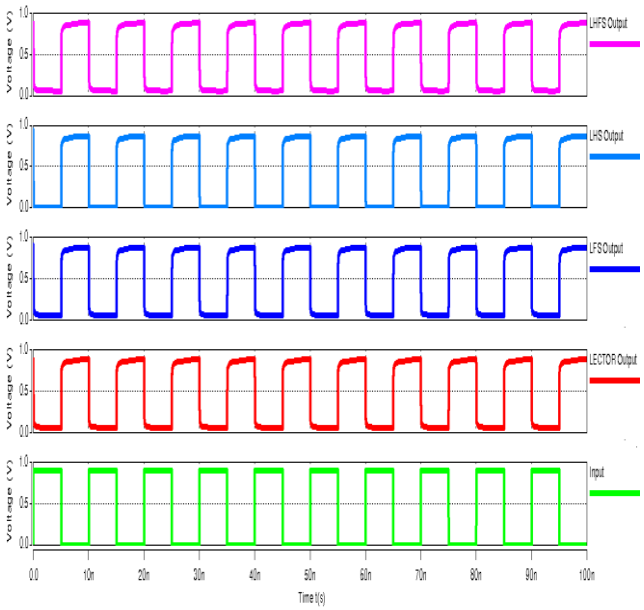

Fig.6: Transient Waveform of existing and Proposed circuit design

IV. RESULTS AND DISCUSSION

There are many existing circuits of leakage is proposed which is compared with over proposed techniques are implemented in CMOS technology. All simulations are performed at 32nm technology using Berkeley Predictive Technology Model (BPTM) with supply voltage of 0.9V, output capacitance C_L=1pF and temperature 25^0C and 110^0C we have kept W/L ratio is 4 for pull up network and 2 for pull down network for fair comparison of results. Leakage power dissipation is calculated (in nanowatts) when no switching activity is measured in all combination of input vector as shown in Table I, II and III. While inserting the two transistor increases the resistance of the circuit without sacrificing the performance the sleep transistor disconnect from V_{DD} to GND and save leakage power. Delay of DVT logic circuits has been increases because of high Vth transistor is used in noncritical path which sprees the overall power flow with delay penalty as shown in Table.II. Static power improvement of 4.43%, -1.23%, 4.43%, 2.36% and 3.16% for DOIND, dual Vth domino, dual Vth DOIND, sleep switch dual Vth and sleep switch dual Vth DOIND approach whereas 45.46%, 67.7%, 68.29%, 99.79% and 99.81% average static power improvement for DOIND.

Table I. Overall Dynamic Power Dissipation 32nm Technology

Techniques	**Dynamic Power (µW)**		**Delay (ps)**		**PDP (aWS)**	
	Low Vth	High Vth	Low Vth	High Vth	Low Vth	High Vth
NG	0.1425	0.0954	7.815	12.12	1.113	1.156
NGHS	0.1587	0.1084	11.56	18.19	1.834	1.971
NGFS	0.1352	0.0946	10.39	17.06	1.400	1.613
NGHFS	0.1578	0.1125	14.41	23.83	2.273	2.680
LECTOR	0.1232	0.0919	10.35	26.87	1.275	2.468
DHS	0.1357	0.0995	15.29	36.28	2.074	3.609
DFS	0.1246	0.0916	8.388	34.25	1.045	3.137
DHFS	0.1364	0.0824	17.89	42.13	2.440	3.471

Table II. Leakage Power at 32nm 25^0C

Techniques	**Leakage Power (nW)**							
	Low Vth				High Vth			
	00	01	10	11	00	01	10	11
NG	9.453	73.28	73.78	63.61	2.485	19.30	2.488	19.26
NGHS	0.866	2.034	2.035	2.824	0.199	0.254	0.260	0.035
NGFS	4.915	9.448	8.447	15.75	1.191	2.489	2.488	2.411
NGHFS	0.646	0.867	0.867	0.273	0.149	0.199	0.199	0.039
LECTOR	9.432	65.88	66.98	54.29	2.411	16.09	15.99	5.368
DHS	0.851	0.987	0.999	0.277	0.193	0.242	0.250	0.035
DFS	4.897	9.319	9.315	14.72	1.175	2.413	2.410	2.159
DHFS	0.648	0.854	0.849	0.276	0.146	0.197	0.199	0.036

Table III. Leakage Power at 32nm 110^0C

Techniques	**Leakage Power (nW)**							
	Low Vth				High Vth			
	00	01	10	11	00	01	10	11
NG	46.33	60.13	52.43	57.65	10.39	12.98	12.59	12.98
NGHS	9.389	9.729	9.740	9.730	1.733	1.763	1.731	0.149
NGFS	18.35	45.42	46.03	53.99	8.385	11.09	10.97	10.84
NGHFS	8.687	9.393	9.397	0.974	1.661	1.707	1.704	0.153
LECTOR	41.3	52.42	52.37	14.08	10.44	19.35	19.12	14.29
DHS	9.257	9.588	9.589	0.974	1.646	1.668	1.671	0.150
DFS	19.04	45.14	45.25	50.20	7.045	10.14	10.44	13.80
DHFS	8.602	9.262	9.264	0.972	1.593	1.639	1.649	0.150

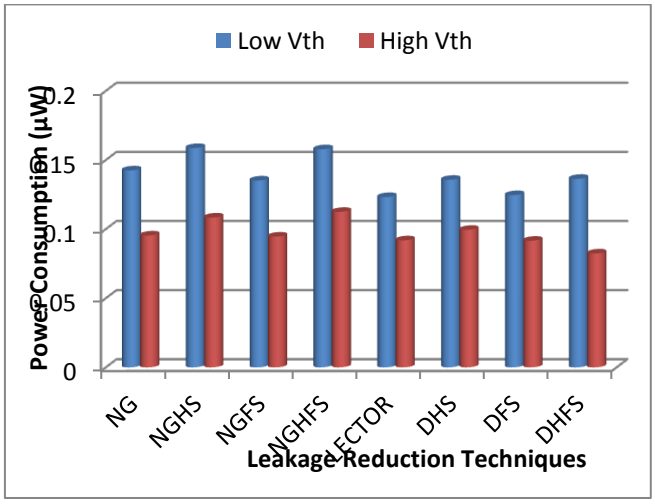

Figure.7: Comparison of Average Power Consumption

For Validation and Verification Circuit is implemented on Full Adder Circuits

V. CONCLUSION

We have proposed a number of techniques for reduction of leakage power there is strong correlation between dynamic power, leakage power and delay of the circuit if optimization of one parameter leads to compromise other parameter. From the results it is observed that DGPT technique gives all the efficient working of the leakage power saving. Overall leakage power improvement of 1q.96% in the proposed DOIND approach, dual Vth DOIND and sleep switch dual Vth DOIND approach whereas 89.72%, 80.12%, 95.27%, 99.96% and 99.98% average leakage current improvement for DOIND, dual Vth domino, dual Vth DOIND, sleep switch dual Vth domino and sleep switch dual Vth DOIND Effect there is little bit variation with increase of the temperature in the proposed sleep DVT DOIND logic circuit as compare to conventional circuit and the proposed circuit is useful for temperature with the digital applications in today's electronics world.

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